REMARKS

Claims 3-21 are pending in this application, with claims 4-10 being independent. Claims 1 and 2 have been canceled and claims 3-10, 11, 12, 14, 16, 18, and 20 have been amended. No new matter is believed to have been introduced. For the reasons set forth below, Applicants respectfully submit that all pending claims as currently amended are patentable over the cited prior art.

Claim Warnings

Claims 16-17 and 20-21 were pointed out as being substantial duplicate of one another. Claim 20 has been amended to remedy this concern.

Claim Rejections – 35 U.S.C. § 112

Claims 12-21 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Claims 12, 14, 16, 18, and 20 have been amended to overcome this objection.

Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 3-5 would be allowable if rewritten in independent form. In reliance on this indication, Applicants have amended claims 3-5 to place them in independent form. Therefore, Applicants respectfully request reconsideration and allowance of these claims at this time.

Claim Rejections – 35 U.S.C. § 103

Claims 1 and 12-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,237,616 ("Abraham") in view of U.S. Patent Number 4,590,552 ("Guttag"). Claim 6 was rejected under § 103(a) as being unpatentable over Abraham, U.S. Patent Number 6,101,586 ("Ishimoto"), U.S. Patent Number 5,414,864 ("Koizumi"). Claims 7, 8, and 10 were rejected under § 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi, U.S. Patent Number 5,680,581 ("Banno"), and U.S. Patent Number 5,386,552 ("Garney"). Claim 9 was rejected under § 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi and Banno. Applicants respectfully traverse these rejections for at least the following reasons. The following remarks first address the rejection of claim 6, then address the rejection of claim 9, and finally addresses the rejections of claims, 7, 8, and 10.

Applicants previously argued that in Abraham user accessible areas are determined based on the privileged mode or the unprivileged mode of the CPU. And, the privileged mode and the unprivileged mode are determined by addresses of data in memory spaces. Abraham at col. 3, lines 5-31. However, Applicants noted that Abraham does not describe or suggest assigning to the data itself a particular mode and storing the data with the particular mode. The Office Action disagrees with Applicants in this regard and asserts that the claim recites storing "data with secure information" without further explaining what the secure information represents or how it is associated with the claimed data. *See e.g.*, Office Action at page 17, lines 4-6.

As such, the Office Action interprets the recitation "secure information" broadly to read on the addresses of data in memory spaces, which determine the privileged or unprivileged state. *See e.g.*, Office Action at page 17, lines 6-9. Furthermore, the Office Action invites Applicants

to clarify what constitutes the "secure information" and how it is linked to the claimed data. *See e.g.*, Office Action at page 17, lines 9-10. Applicants accept this invitation.

To this end and in an effort to place this application in condition for allowance, Applicants have amended claims 6-10 to further clarify what constitutes the "secure information" and how it is linked to the claimed data. In particular, as amended, claim 6 recites an information processing apparatus for accessing memory spaces including a user memory space and a secure memory space. The information processing apparatus includes, among other features, a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, and a built-in RAM space for receiving and holding the data with one or more secure bits from the general purpose register and delivering the data with one or more secure bits to the general purpose register. The information processing apparatus also includes a data output control unit having a function of controlling a data transfer to an external space by using the secure bit.

Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6 because Abraham, Ishimoto, and Koizumi, either alone or in combination, fail to describe or suggest an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, (2) a built-in RAM space for receiving and holding the data with one or more secure bits from the general purpose register and delivering the data with one or more secure bits

to the general purpose register, and (3) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit, as recited in claim 6.

In Abraham, the information processing apparatus permits a computer to be operated in either a privileged state or an unprivileged state. Abraham at Abstract. In the privileged state, the microprocessor works with the privileged memory (105) and no data or addresses of the memory are accessible outside the secure module represented by boundary (101) in FIG. 1. Abraham at col. 2, lines 61-65. In the unprivileged state, the microprocessor works only with memory (109) and data, addresses, and programs in the privileged memory (105) is made unavailable. Abraham at col. 2, lines 65-67.

As such, Abraham describes an information processing in which addresses of data in memory spaces determine privileged or unprivileged states. Even assuming for the sake of argument that the alleged addresses of data correspond to the secure information recited in claim 6, Abraham does not describe or otherwise suggest that secure bits are produced from the secure information, that the secure bits are appended to data itself on a bit basis when transferring the data, and that the general purpose register and the built-in memory are configured to hold the secure bits appended to data.

Accordingly, Abraham fails to describe or suggest an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, (2) a built-in RAM space for receiving and holding the data with one or more secure bits from the general purpose register and delivering the data with one or more secure bits to the general purpose

register, and (3) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit, as recited in claim 6.

The distinction is one of the important features of the present application (e.g., data management by appending secure bits to each data accessed). In particular, because secure bits is appended to each data accessed when arithmetic operation or data transfer is performed through a general purpose register or a built-in memory, data does not need to be protected by a privileged mode or privileged status, and access is not limited according to the types of memory spaces. This can provide several advantages. For example, in a secure memory space, easier data access and arithmetic operation using a program in a user memory space can be achieved. This is quiet an improvement over Abraham and other cited references.

Ishimoto and Koizumi also fail to describe or suggest the above-recited feature of claim 6. Ishimoto relates to a memory access control circuit for inhibiting fraudulent access by detecting an access to a region to be protected on a memory. Ishimoto at col. 12, lines 36-39. The memory access control circuit includes address of data region in the memory that must be protected. Ishimoto at col. 12, lines 43-44. And, if the instructions seek to access this data region, the memory access control checks to determine whether the location of the instruction is within a region in the memory that allows access to the protected region. Ishimoto at col. 12, lines 45-67.

As such, Ishimoto describes a memory access control that provides protection depending on areas where the data is allocated. That is access to the secured memory is only possible by instructions stored in a particular area in the memory. In contrast and as described below in more detail, the protection mechanism of claim 6, does not limit access based on areas. Rather,

in claim 6, the one or more secure bits delivered with the data limits the output of the respective data to an external space.

Accordingly, Ishimoto fails to describe or suggest an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, (2) a built-in RAM space for receiving and holding the data with one or more secure bits from the general purpose register and delivering the data with one or more secure bits to the general purpose register, and (3) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit, as recited in claim 6.

Koizumi also fails to describe or suggest the above-recited features of claim 6. The purpose of Koizumi's invention is to save/store registers using flags that indicate whether or not the register set is being used. Koizumi at col. 2, lines 31-42. These protective flags are not added to data but to the register set upon instructions to start/stop use of registers. To this end, Koizumi is not seen to have an association with security. Furthermore, the alleged general purpose register in Koizumi does not appear to have any secure bit appended thereto.

Accordingly, Koizumi also fails to describe or suggest an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, (2) a built-in RAM space for receiving and holding the data with one or more secure bits from the

general purpose register and delivering the data with one or more secure bits to the general purpose register, and (3) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit, as recited in claim 6.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6.

Claim 9 was rejected under § 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi and Banno. Applicants respectfully traverse this rejection.

Claim 9 recites an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information and delivering data with one or more secure bits into the DMA, (2) a built-in RAM space for receiving and holding the data with one or more secure bits from the DMA, and (3) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit.

Banno fails to remedy the shortcomings of Abraham, Ishimoto, and Koizumi to describe or suggest the above-recited features of claim 9. Banno describes protecting data read from CPU. Similar to Ishimoto, Banno data protection/non protection is also executed depending on areas where data is located. *See e.g.,* Banno at col. 3, lines 44-61. As such, Banno also fails to describe or suggest limiting the output of the respective data to an external space by delivering the data with one or more secure bits. For at least this reason, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 9.

Claims 7, 8, and 10 were rejected under § 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi, Banno, and Garney. Applicants respectfully traverse this rejection for the following reasons.

Claim 7 recites an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits; (2) a built-in RAM space with a secure bit for receiving and holding the data with one or more secure bits from the general purpose register, (3) an interrupt saved information unit with a secure bit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space, and (4) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit.

Applicants respectfully submit that Garney fails to remedy shortcomings of Abraham, Ishimoto, and Koizumi to describe or suggest the above-recited features. Garney is intended for efficient preservation of CPU's processing state in a computer system with volatile memories and registers. Garney is not seen to describe or suggest anything about securing data, much less describing adding secure bit to the data saved in a stack area of the built-in memory of the built-in RAM and controlling a data transfer to an external space by using the security bit, as recited in claim 7. For at least this reason, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 7.

Claim 8 recites an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, (2) a built-in RAM space with a secure bit having a

function of receiving and holding the data with one or more secure bits from the general purpose register, and (3) an interrupt saved information unit with a secure bit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space. Therefore, for at least the reasons presented above with respect to claim 7, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 8.

Claim 10 recites an information processing apparatus that includes, among other features, (1) a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits, (2) an operating unit with a secure bit having a function of reflecting the secure bits of the instruction decoder in an arithmetic operation executed in accordance with the instruction decoded by the instruction decoder, and (3) a data output control unit having a function of controlling a data transfer to an external space by using the secure bit. Therefore, for at least the reasons presented above with respect to claim 7, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 10.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 6-10 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In

addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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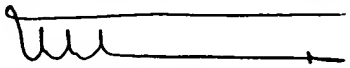

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